

NX20P5090

High voltage USB PD power switch

Rev. 1 — 14 October 2016

Product data sheet

1. General description

The NX20P5090 is an advanced 5 A unidirectional power switch for USB PD. It includes under voltage lockout, over voltage lockout, reverse current protection and over-temperature protection circuits. It is designed to automatically isolate the power switch terminals when a fault condition occurs. Both VBUS and VINT pins have 29 V tolerance in shutdown mode. Two NX20P5090 chips can be used in parallel to support dual power inputs connecting to the same charging circuit.

The device has a default 23 V over voltage protection threshold, and the OVP threshold can be adjusted by using an external resistor divider on OVLO pin. A 15 ms de-bounce time is deployed every time before the device is switched ON, followed by a soft start to limit the inrush current.

Designed for operation from 2.5 V to 20 V, it is used in USB PD power control applications to offer essential protection and enhance system reliability.

NX20P5090 is offered in a small 15 bump, 2.56 x 1.54 x 0.555 mm WLCSP package.

2. Features and benefits

- Wide supply voltage range from 2.5 V to 20 V
- I_{SW} maximum 5 A continuous current
- 29 V tolerance on both VBUS and VINT pin
- 30 m Ω (typical) Low ON resistance
- Adjustable VBUS over voltage protection
- Built in slew rate control for inrush current limit
- All time two level reverse-current protection
- Protection circuitry
 - ◆ Over-Temperature Protection
 - ◆ Over-Voltage Protection
 - ◆ Under-Voltage Lockout
 - ◆ Reverse Current Protection
- Surge protection:
 - ◆ IEC61000-4-5 exceeds ± 90 V on VBUS without capacitor
 - ◆ IEC61000-4-5 exceeds ± 100 V on VBUS with 22 μ F capacitor



- ESD protection
 - ◆ IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - ◆ CDM AEC standard Q100-01 (JESD22-C101E)
- Specified from -40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks
- Notebooks

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX20P5090UK	-40 °C to +85 °C	WLCSP15	wafer level chip-scale package; 15 bumps; 2.56 x 1.54 x 0.555 mm (Backside coating included)	SOT1392-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
NX20P5090UK	NX20P5090UKAZ	WLCSP15	REEL 7" Q2/T3 *SPECIAL MARK CHIPS DP	3000	T _{amb} = -40 °C to +85 °C

5. Marking

Table 3. Marking

Line	Marking	Description
A	X20PPD	basic type name
B	mmmmmmnn	wafer lot code (mmmmmm) and wafer number (nn)
C	ZtDYYWW	manufacturing code: Z = foundry location t = assembly location D = RoHS code (dark green) YY = assembly year code WW = assembly week code

6. Functional diagram

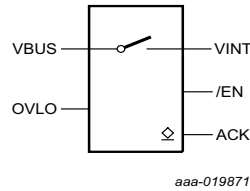


Fig 1. Logic symbol

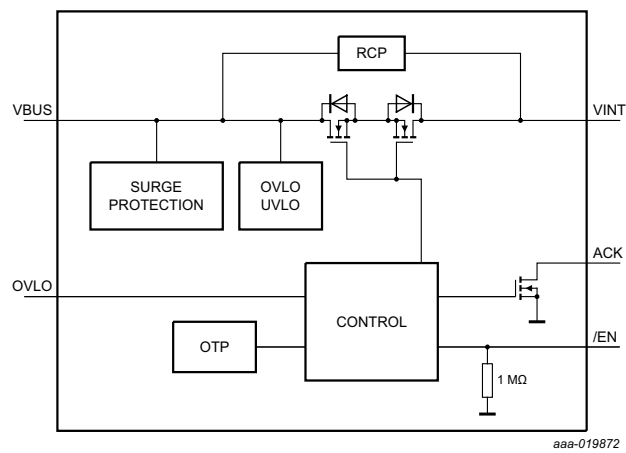


Fig 2. Logic diagram

7. Pinning information

7.1 Pinning

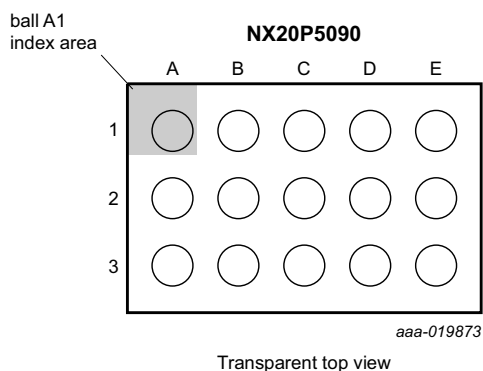


Fig 3. Pin configuration WLCSP15

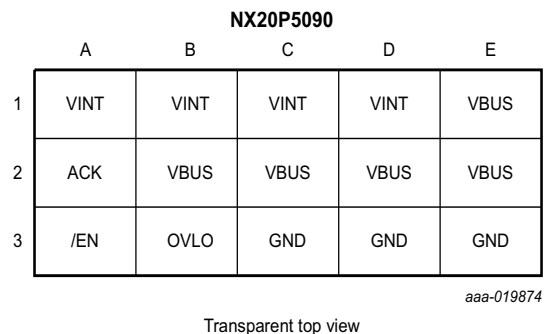


Fig 4. Ball mapping for WLCSP15

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VBUS	B2, C2, D2, E1, E2	VBUS (Power Input)
VINT	A1, B1, C1, D1	VINT (Power Output)
OVLO	B3	V_{OVLO} threshold input
ACK	A2	Power Good Acknowledge (open-drain output)
GND	C3, D3, E3	ground (0 V)
$\overline{\text{EN}}$	A3	enable input (active LOW)

8. Functional description

Table 5. Function table^[1]

$\overline{\text{EN}}$	VBUS	VINT	ACK	Operation mode
L	< 2.5 V	X	Z	Under-voltage lockout; switch open
L	2.5 V < VBUS < V _{OVLO}	X	L	Enabled; switch closed; charging mode
L	X	X	Z	Over-temperature protection; switch open
L	> V _{OVLO}	X	Z	Over-voltage lockout; switch open
H	X	X	Z	Disable; switch open
X	X	VINT > VBUS	Z	Reverse Current Protection; Switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.1 $\overline{\text{EN}}$ -input

A HIGH on $\overline{\text{EN}}$ disables the channel MOSFET and all protection circuits, putting the device into low power mode. A LOW on $\overline{\text{EN}}$ enables the protection circuits and the MOSFET. There is an internal 1 M Ω pull-down resistor on the $\overline{\text{EN}}$ pin to ensure the power switch conduction in a dead-battery situation. A 15 ms de-bounce time has been deployed before device turn-on. $\overline{\text{EN}}$ pin has 29 V tolerance.

8.2 Under-voltage lockout

When $\overline{\text{EN}}$ is LOW and VBUS < V_{UVLO}, the Under-Voltage LockOut (UVLO) circuits disable the power MOSFET. Once VBUS exceeds V_{UVLO} and no other protection circuit is active, the channel MOSFET state is controlled by the $\overline{\text{EN}}$ pin.

8.3 Over-voltage lockout

When $\overline{\text{EN}}$ is LOW and VBUS > V_{OVLO}, the over-voltage lockout (OVLO) circuit disables the power MOSFET. Once VBUS drops below V_{OVLO} and no other protection circuit is active, the power MOSFET resumes operation.

OVLO pin is used to set the over-voltage threshold. The default over-voltage threshold is 23 V when OVLO pin shorts to GND. Connecting a resistor divider to the OVLO pin (see [Figure 5](#)) adjusts the over voltage threshold from 4 V to 23 V using [Equation 1](#):

$$V_{ovlo} = V_{th(ovlo)} \times (R1 + R2) / (R2) \quad (1)$$

When the voltage on OVLO pin is below 0.1 V, the device defaults to the 23 V OVP threshold.

8.4 Over-temperature protection

When $\overline{\text{EN}}$ is LOW and the device temperature exceeds 140 °C the Over-Temperature Protection (OTP) circuit disables the power MOSFET and sets the ACK output Hi-Z. Once the device temperature decreases below 115 °C and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the $\overline{\text{EN}}$ pin again.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. The ACK pin indicates the state of the power switch. When no fault is detected and power switch is conducting, ACK goes output low, otherwise it stays at high impedance. The pull up resistor value is recommend to be 10 KΩ to 200 KΩ.

8.6 Reverse Current Protection

NX20P5090 has all time reverse current protection regardless of the \overline{EN} logic level. Once the voltage on VINT is higher than VBUS for 45 mV, the RCP circuit is triggered after a 3.7ms de-glitch time. If the voltage gap is greater than 120 mV, RCP triggers immediately to switch off the power MOSFET.

During the start up de-glitch time, if the device detects the VINT voltage is higher than VBUS by 45 mV, the power MOSFET does not turn on.

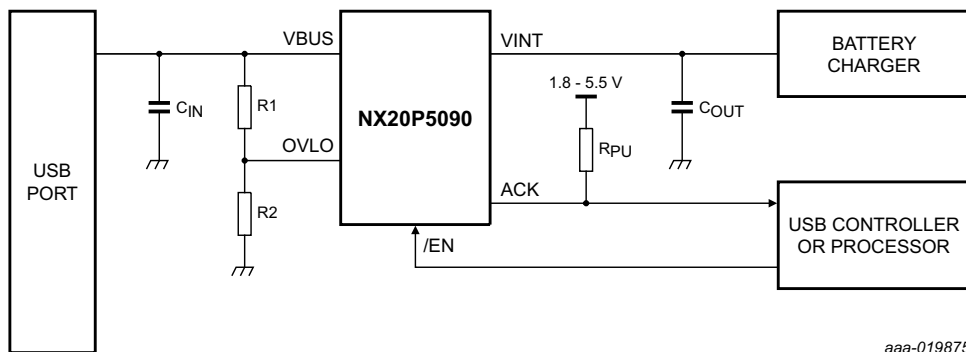
The RCP circuit helps by providing the capability of parallel connection of two USB charging ports to a single charger input, without backward leakage.

9. Application diagram

The NX20P5090 is typically used on a USB port charging path in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level that it is connected to.

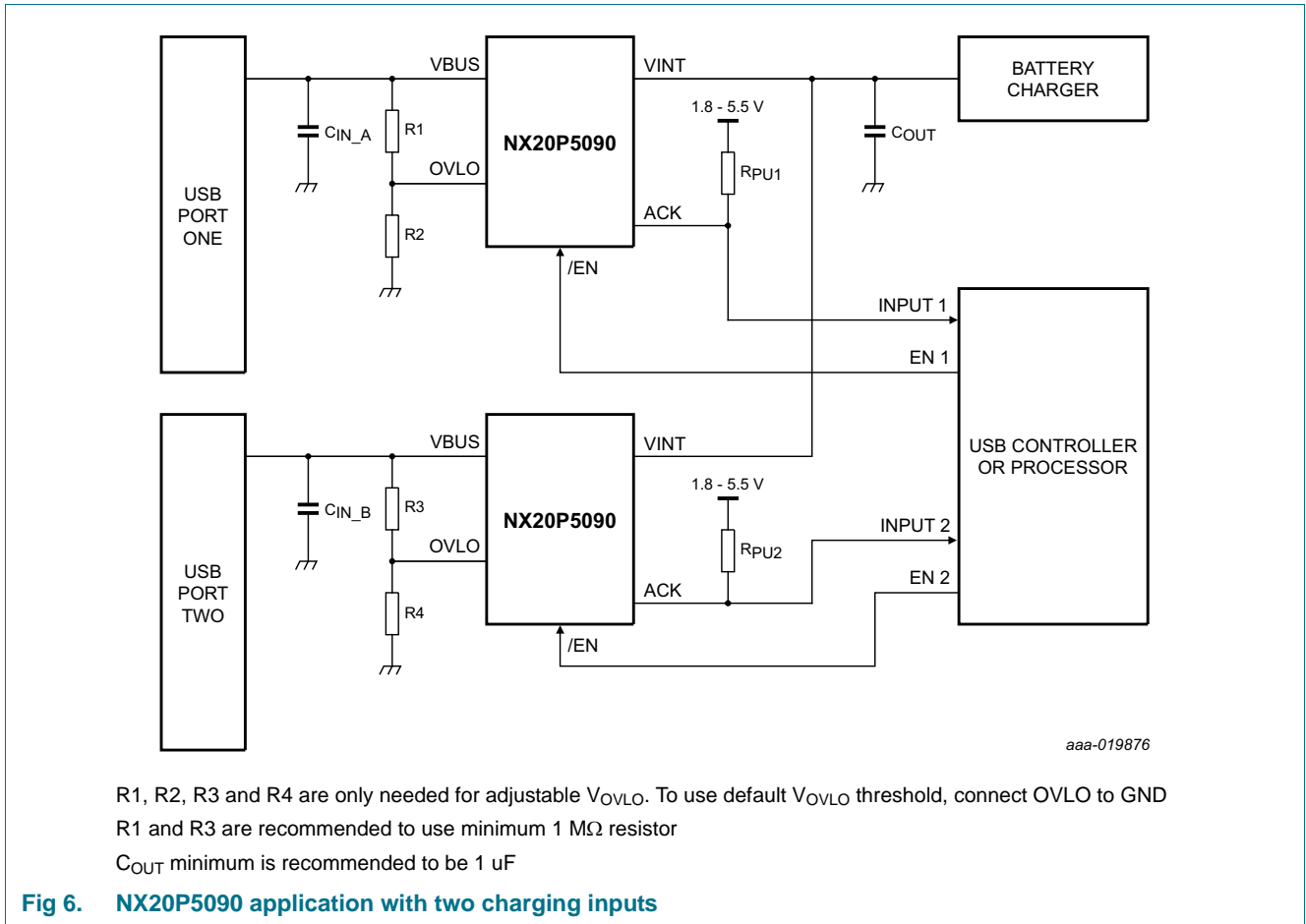
When the default 23 V OVP threshold is used, the OVLO pin shorts to GND. If an adjustable OVP threshold is needed, a resistor divider is connected to the OVLO pin.

For best performance, it is recommended to keep input and output traces short and capacitors as close to the device as possible. Regarding thermal performance, it is recommended to increase the PCB area around VINT and VBUS pins.



R1 and R2 are only needed for adjustable V_{OVLO} ; to use default V_{OVLO} threshold, connect OVLO to GND
 R1 is recommended to use minimum 1 MΩ resistor
 C_{OUT} minimum is recommended to be 1 uF

Fig 5. NX20P5090 application with one charging input



10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_i	input voltage	VBUS	[1] -0.5	+29	V
		VINT	[1] -0.5	+29	V
		OVLO	-0.5	VBUS	V
		\overline{EN}	[2] -0.5	+29	V
V_o	output voltage	ACK	-0.5	+6.0	V
I_{IK}	input clamping current	\overline{EN} : $V_i < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	VBUS; VINT; $V_i < -0.5$ V	-50	-	mA
I_{SW}	continuous switch current	$T_{amb} = 85$ °C	-	5	A
		$T_{amb} = 105$ °C	-	3.5	A
	peak switch current	100 μ s pulse, 2% duty cycle	-	10	A
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	-	1.45	W

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	VBUS	2.5	20	V
		VINT	2.5	20	V
		$\overline{\text{EN}}$	0	20	V
V _O	output voltage	ACK	0	5.5	V
T _{j(max)}	maximum junction temperature		-40	+125	°C
T _{amb}	ambient temperature		-40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient		[1][2] 67.2	K/W

- [1] The overall R_{th(j-a)} can vary depending on the board layout. To minimize the effective R_{th(j-a)}, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.
- [2] This R_{th(j-a)} is calculated based on JEDEX2S2P board. The actual R_{th(j-a)} value may vary in applications using different layer stacks and layouts.

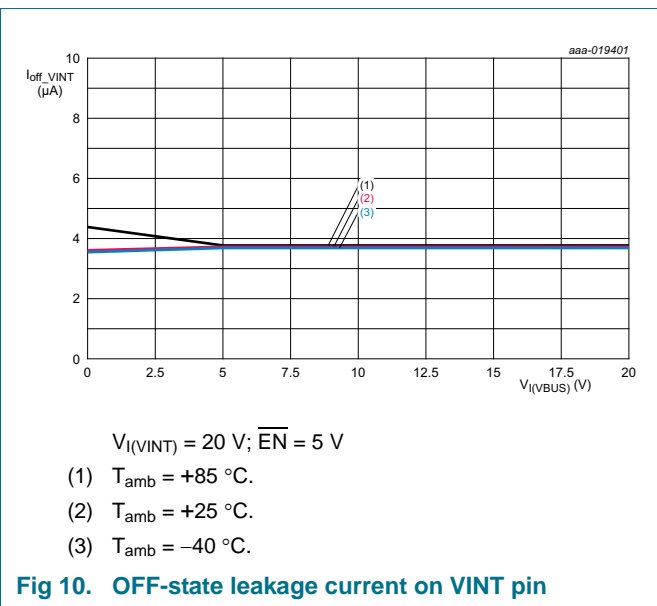
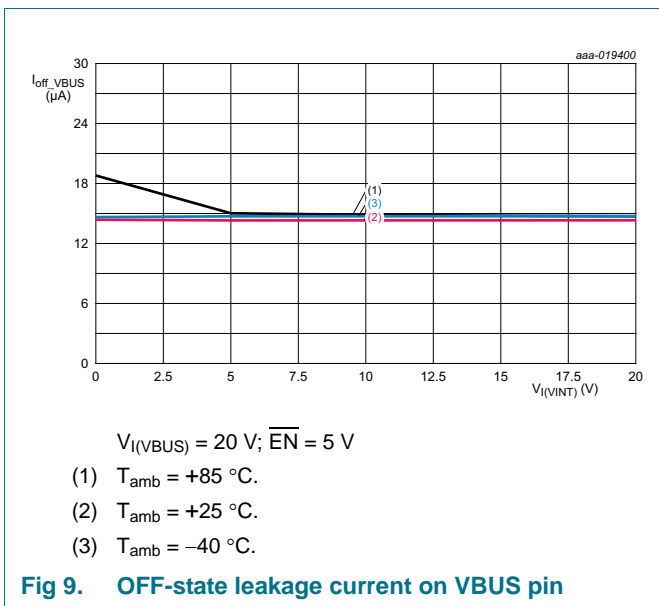
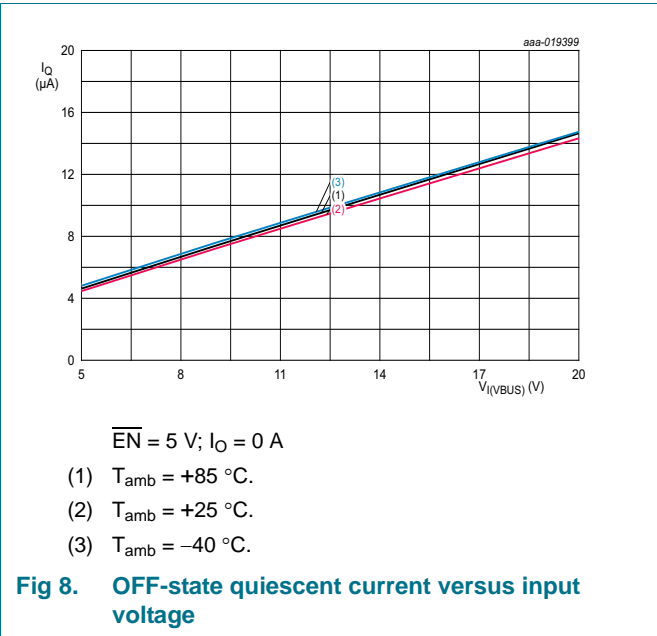
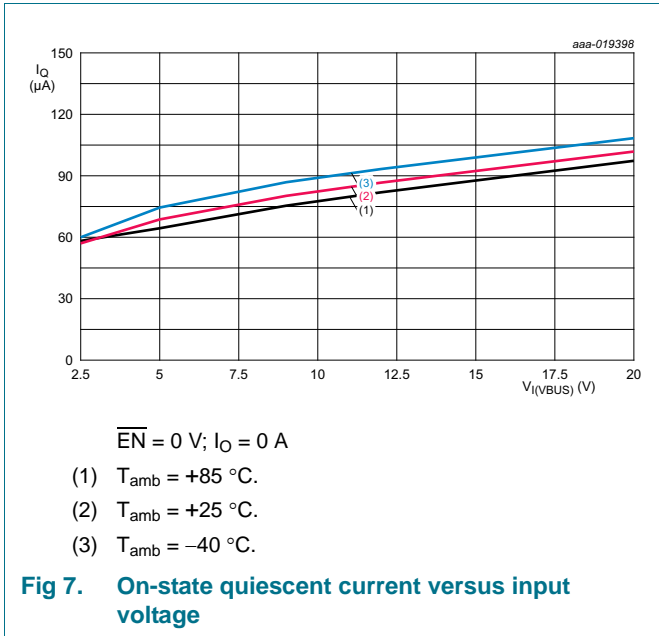
13. Static characteristics

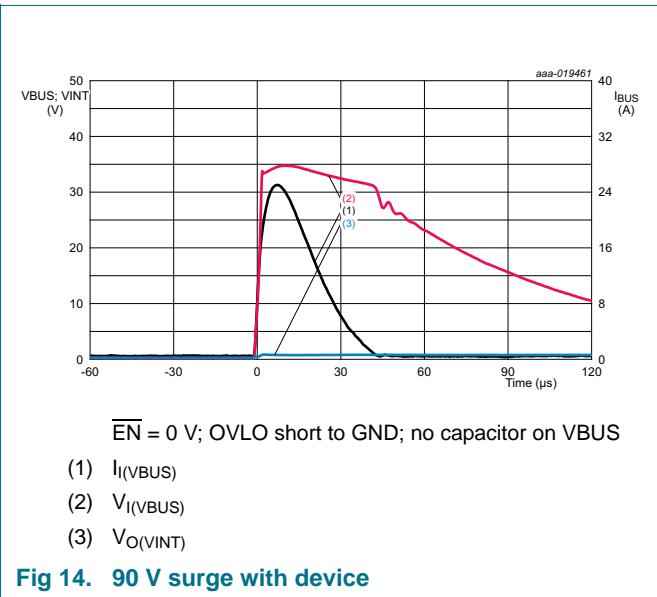
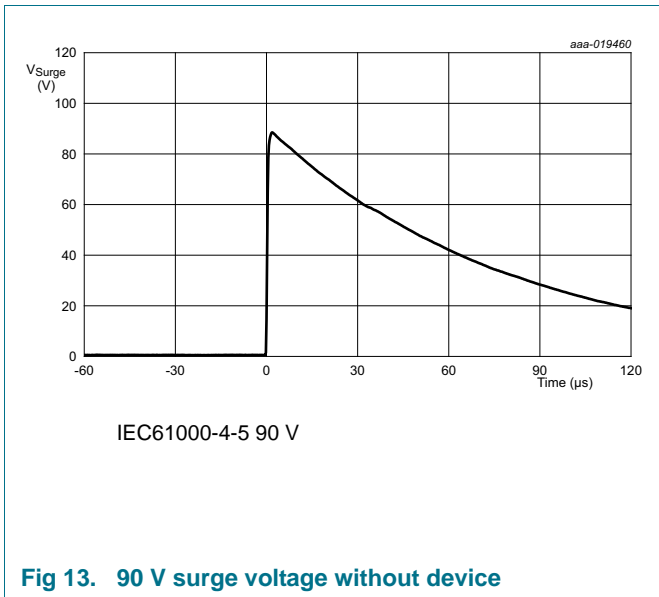
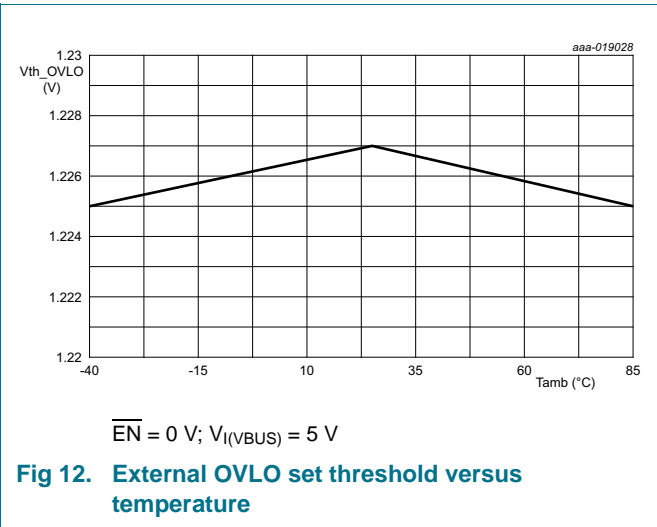
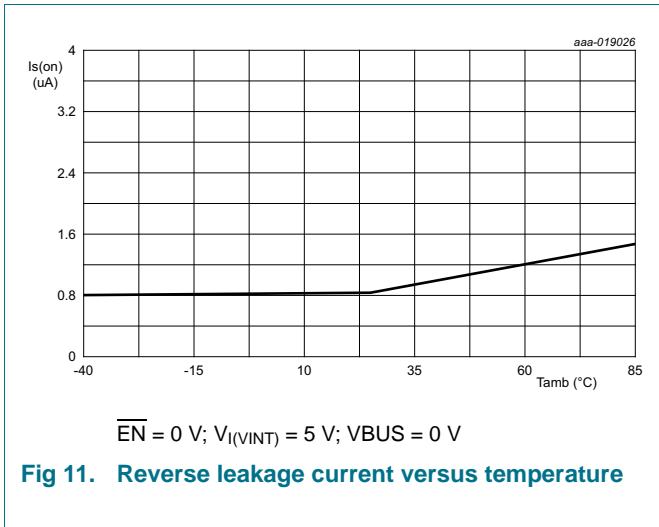
Table 9. Static characteristics

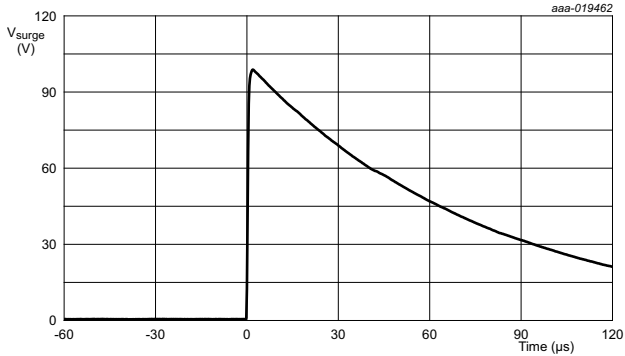
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{IH}	HIGH-level input voltage	\overline{EN} pin; V _{I(VBUS)} = 2.5 V to 20 V	1.2	-	-	1.2	-	V
V _{IL}	LOW-level input voltage	\overline{EN} pin; V _{I(VBUS)} = 2.5 V to 20 V	-	-	0.4	-	0.4	V
V _{OL}	LOW-level output voltage	ACK; I _O = 8 mA; V _{I(VBUS)} = 2.5 V to 20 V	-	-	0.5	-	0.5	V
R _{pd}	pull-down resistance	\overline{EN}	-	1	-	-	-	MΩ
I _q	VBUS quiescent current	\overline{EN} = 0 V; V _{I(VBUS)} = 5.0 V; I _O = 0 A;	-	70	-	-	95	μA
		\overline{EN} = 0 V; V _{I(VBUS)} = 20 V; I _O = 0 A;	-	100	-	-	140	μA
		\overline{EN} = 5.0 V; V _{I(VBUS)} = 5.0 V; I _O = 0 A;	-	5	-	-	10	μA
		\overline{EN} = 5.0 V; V _{I(VBUS)} = 20 V; I _O = 0 A;	-	15	-	-	30	μA
I _{S(OFF)}	VBUS OFF-state leakage current	\overline{EN} = 5.0 V; V _{I(VBUS)} = 5.0 V; V _{INT} = 0 V	-	5	-	-	10	μA
		\overline{EN} = 5.0 V; V _{I(VBUS)} = 20 V; V _{INT} = 0 V	-	15	-	-	30	μA
	VINT OFF-state Leakage current	\overline{EN} = 5.0 V; V _{I(VINT)} = 5.0 V; VBUS = 0 V	-	1	-	-	5	μA
		\overline{EN} = 5.0 V; V _{I(VINT)} = 20 V; VBUS = 0 V	-	4	-	-	16	μA
I _{S(ON)}	RCP leakage current	\overline{EN} = 0 V; V _{I(VINT)} = 5 V; V _(VBUS) = 0 V	-	1	-	-	5	μA
I _I	OVLO input leakage Current	V _{OVLO} = V _{th(OVLO)}	-	-	-	-	50	nA
V _{UVLO}	under-voltage lockout release voltage	VBUS Rising; \overline{EN} = 0 V	-	2.37	-	2.24	2.5	V
V _{hys(UVLO)}	under-voltage lockout hysteresis voltage	VBUS Falling	-	100	-	-	-	mV
V _{OVLO}	Default overvoltage lockout voltage	VBUS Rising; \overline{EN} = 0 V; OVLO short to GND	-	23	-	-	-	V
		VBUS Falling; \overline{EN} = 0 V; OVLO short to GND	-	22.5	-	-	-	V
V _{th(OVLO)}	external OVLO set threshold voltage	V _{I(VBUS)} = 2.5 V to 20 V; \overline{EN} = 0 V	-	1.227	-	1.164	1.287	V
V _{trig}	RCP trigger voltage	V _{trig} = V _(VINT) - V _(VBUS)	-	45	-	10	80	mV
C _I	input capacitance	\overline{EN} pin; V _{I(VBUS)} = 5 V	-	4.5	-	-	-	pF

13.1 Graphs

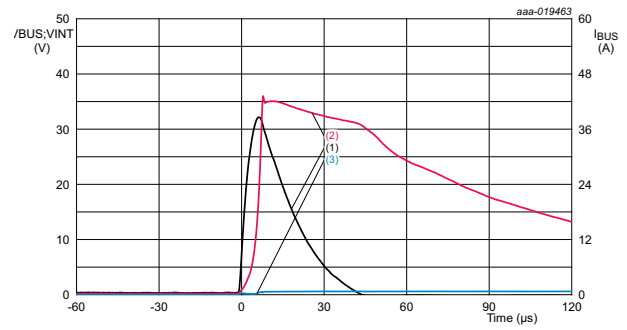






IEC61000-4-5 100 V

Fig 15. 100 V surge voltage without device



$\overline{EN} = 0$ V; OVLO short to GND; 22 μ F capacitor on VBUS

- (1) $I_{I(VBUS)}$
- (2) $V_{I(VBUS)}$
- (3) $V_{O(VINT)}$

Fig 16. 100 V surge with device

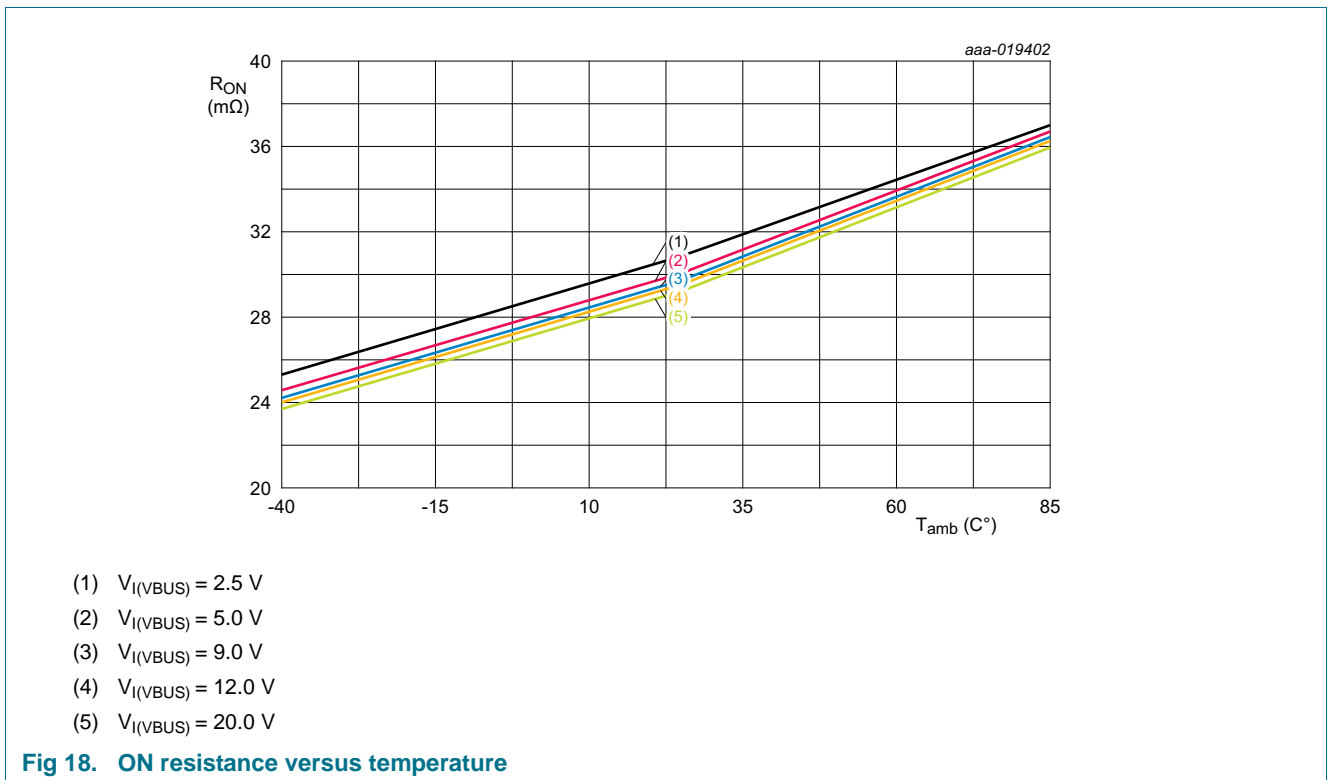
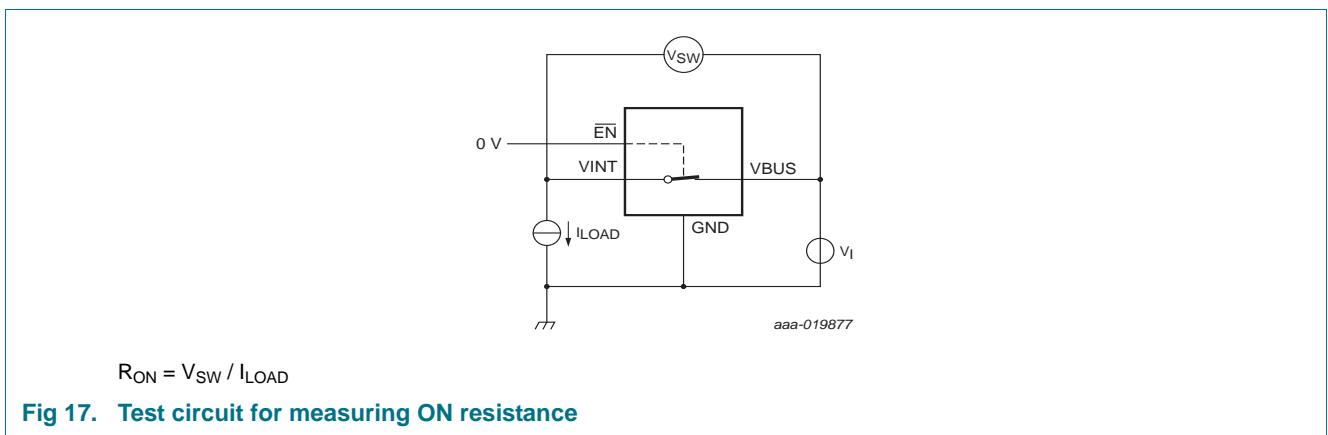
13.2 ON resistance

Table 10. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R _{ON}	ON resistance	I _{LOAD} = 1 A						
		V _{I(VBUS)} = 5.0 V	-	30	36	-	43	mΩ
		V _{I(VBUS)} = 20 V	-	30	36	-	43	mΩ

13.3 ON resistance test circuit and graphs



14. Dynamic characteristics

Table 11. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 20](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t _{en}	Enable Time	From $\overline{\text{EN}}$ to V _(VINT) = 10% of V _(VBUS) ; (Including 15ms debounce time); V _{I(VBUS)} = 5 V; C _{Load} = 100μF; R _{Load} = 100Ω	-	21.9	-	-	-	ms
t _{TLH}	VINT rise time	V _(VINT) from 10% to 90% V _(VBUS) ; C _{Load} = 100μF; R _{Load} = 100Ω						
		V _{I(VBUS)} = 5 V	-	3.4	-	-	-	ms
		V _{I(VBUS)} = 20 V	-	6.9	-	-	-	ms
t _{dis(OVP)}	OVP turn off time	From V _(VBUS) > V _{ovlo} to V _(VINT) = 80% of V _(VBUS) ; R _{load} = 100Ω; C _{load} = 0 μF; V _{I(VBUS)} = 20 V; OVLO pin short to GND	-	122	-	-	-	ns
t _{degl}	RCP de-glitch time	From V _(VINT) > V _(VBUS) + 45mV to switch off	-	3.7	-	2.6	4.8	ms
t _{dis(RCP)}	RCP turn off time	From V _(VINT) > V _(VBUS) + 120mV to switch off	[1]	10	-	-	-	us
t _{on}	turn-on time	$\overline{\text{EN}}$ to V _(VINT) = 90% V _(VBUS)						
		V _{I(VBUS)} = 5.0 V	-	25.3	-	-	-	ms
		V _{I(VBUS)} = 20 V	-	29.2	-	-	-	ms
t _{off}	turn-off time	$\overline{\text{EN}}$ to V _(VINT) = 10% V _(VBUS)						
		V _{I(VBUS)} = 5.0 V; C _{Load} = 100μF; R _{Load} = 100Ω	-	23	-	-	-	ms
		V _{I(VBUS)} = 20 V; C _{Load} = 100μF; R _{Load} = 100Ω	-	23	-	-	-	ms

[1] Guaranteed by design

14.1 Waveforms and test circuit

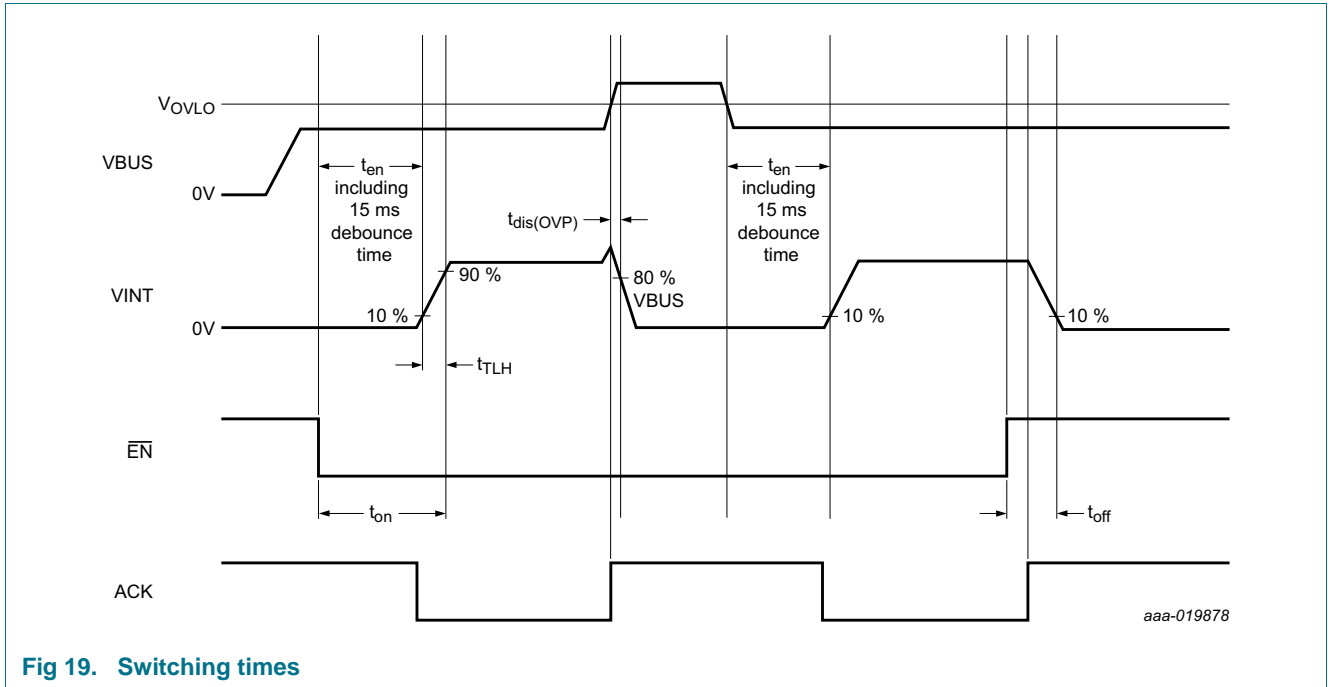


Fig 19. Switching times

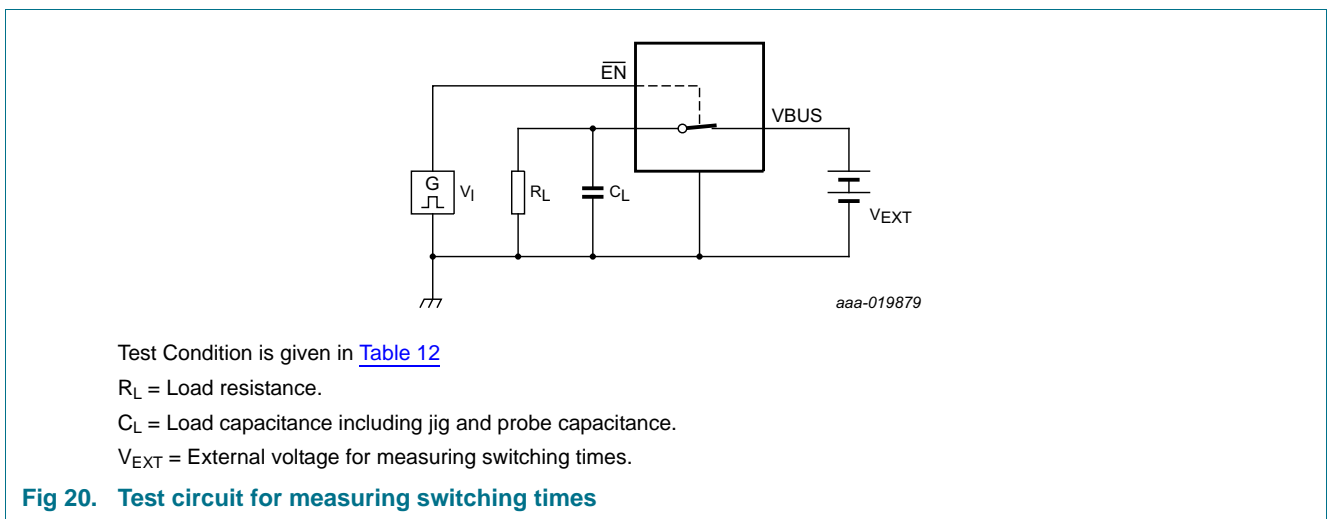
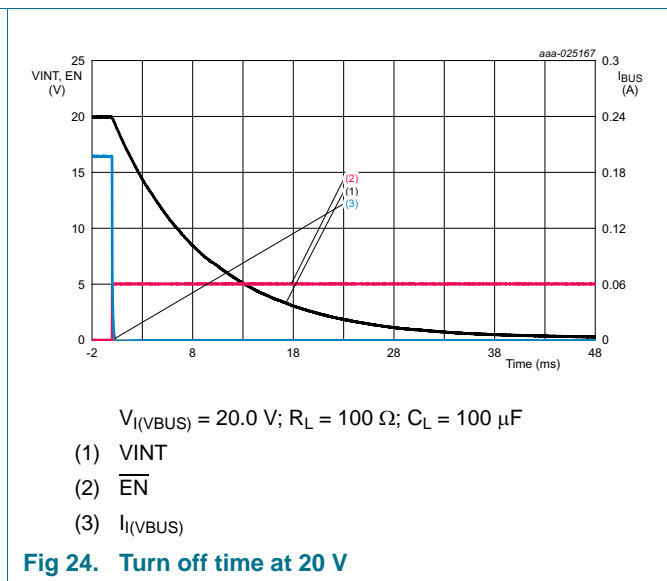
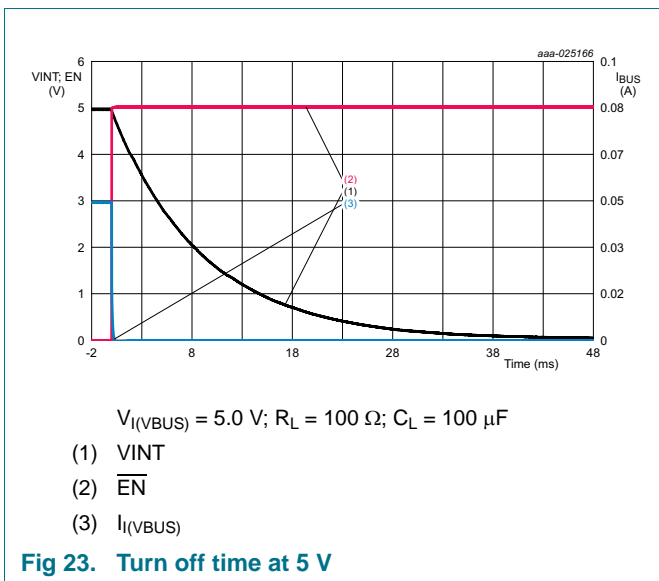
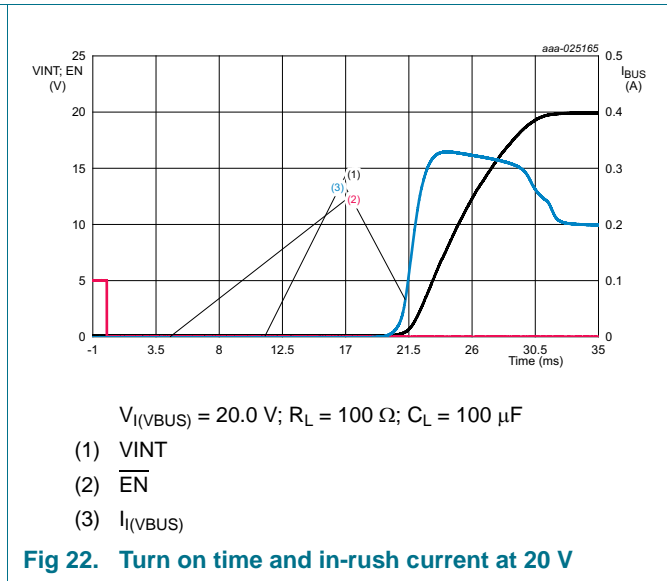
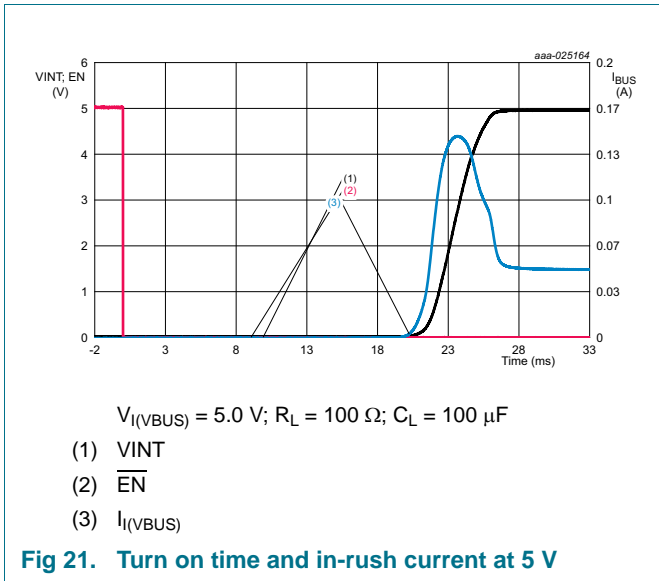


Fig 20. Test circuit for measuring switching times

Table 12. Test Condition

Supply voltage V _{EXT}	Load	
VBUS	C _L	R _L
2.5 V to 20 V	100 μF	100 Ω



15. Package outline

WLCSP15: wafer level chip-scale package; 15 bumps; 2.56 x 1.54 x 0.555 mm (Backside coating included)

SOT1392-1

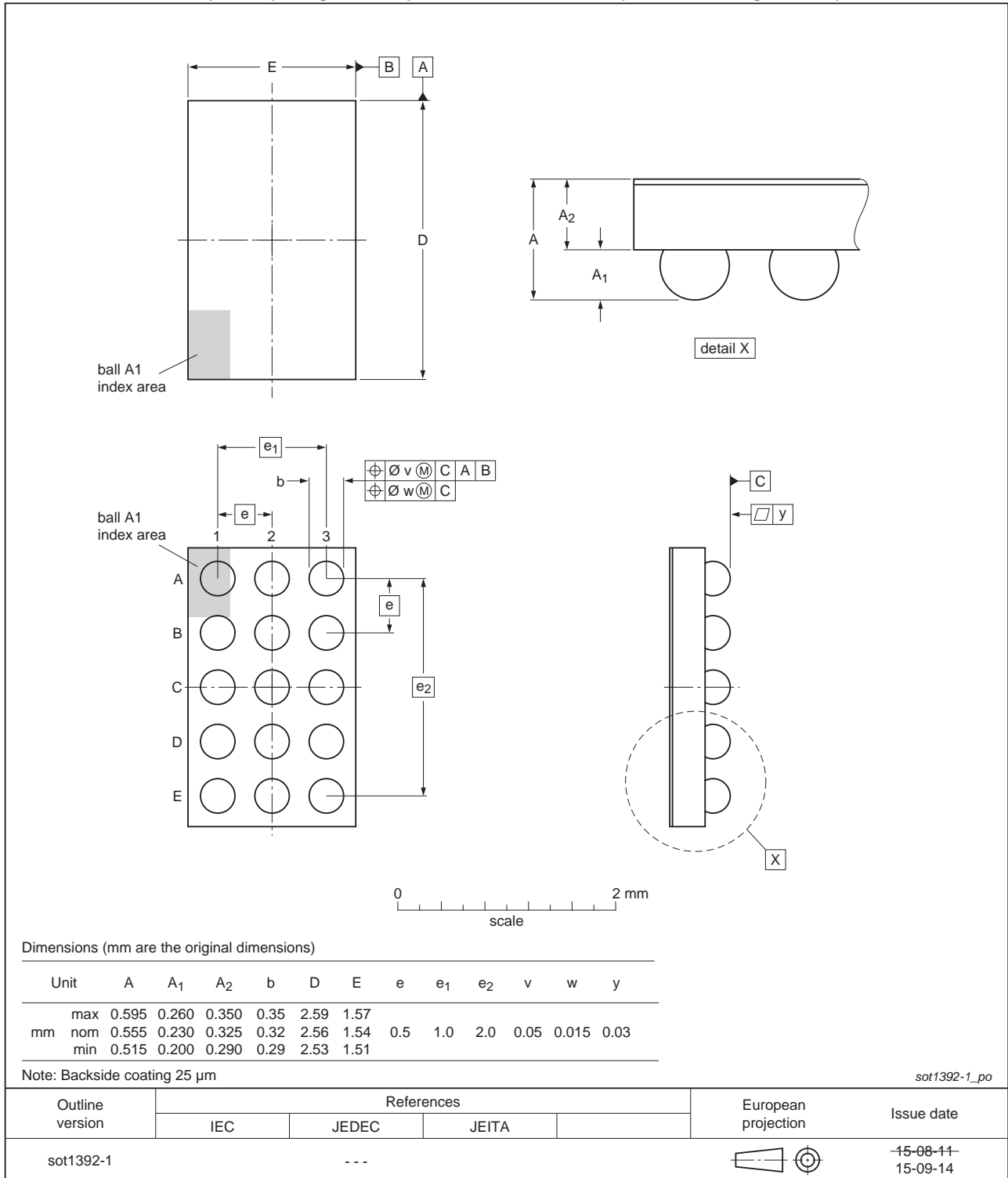


Fig 25. Package outline SOT1392-1 (WLCSP15)

16. Packing information

16.1 Packing method

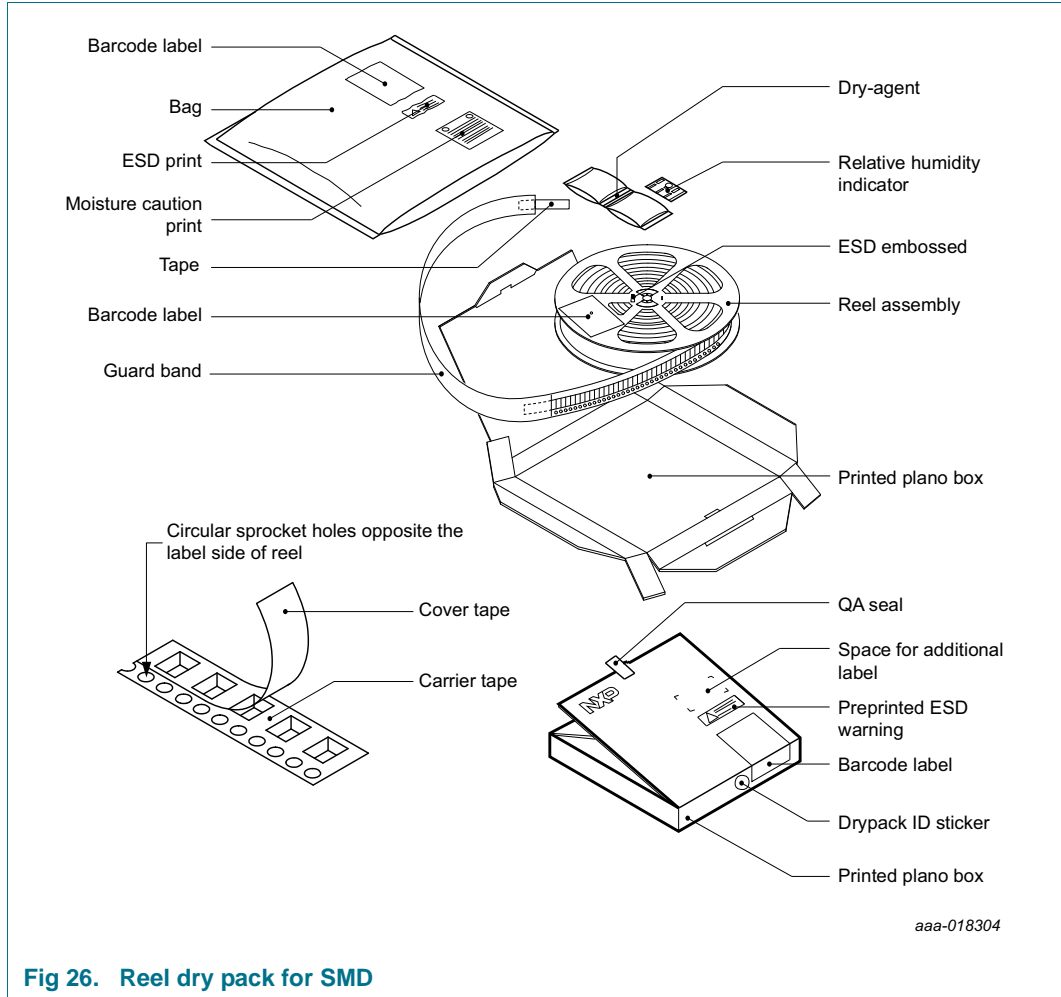


Table 13. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
180 × 12	3000	1	209 × 206 × 37

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.

View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

16.2 Product orientation



16.3 Carrier tape dimensions

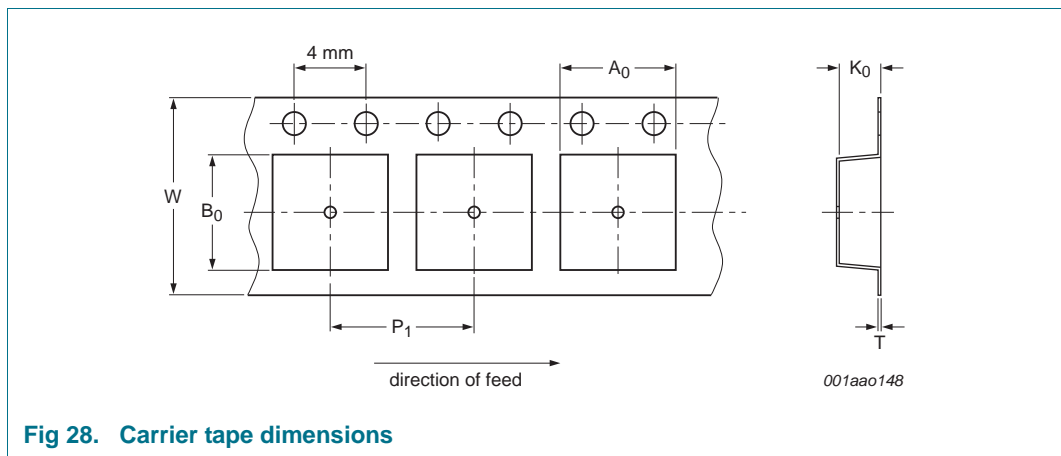


Table 14. Carrier tape dimensions

In accordance with IEC 60286-3.

A₀ (mm)	B₀ (mm)	K₀ (mm)	T (mm)	P₁ (mm)	W (mm)
1.67 ± 0.05	2.69 ± 0.05	0.70 ± 0.05	0.25 ± 0.02	4.0 ± 0.1	12 + 0.3 / - 0.1

16.4 Reel dimensions

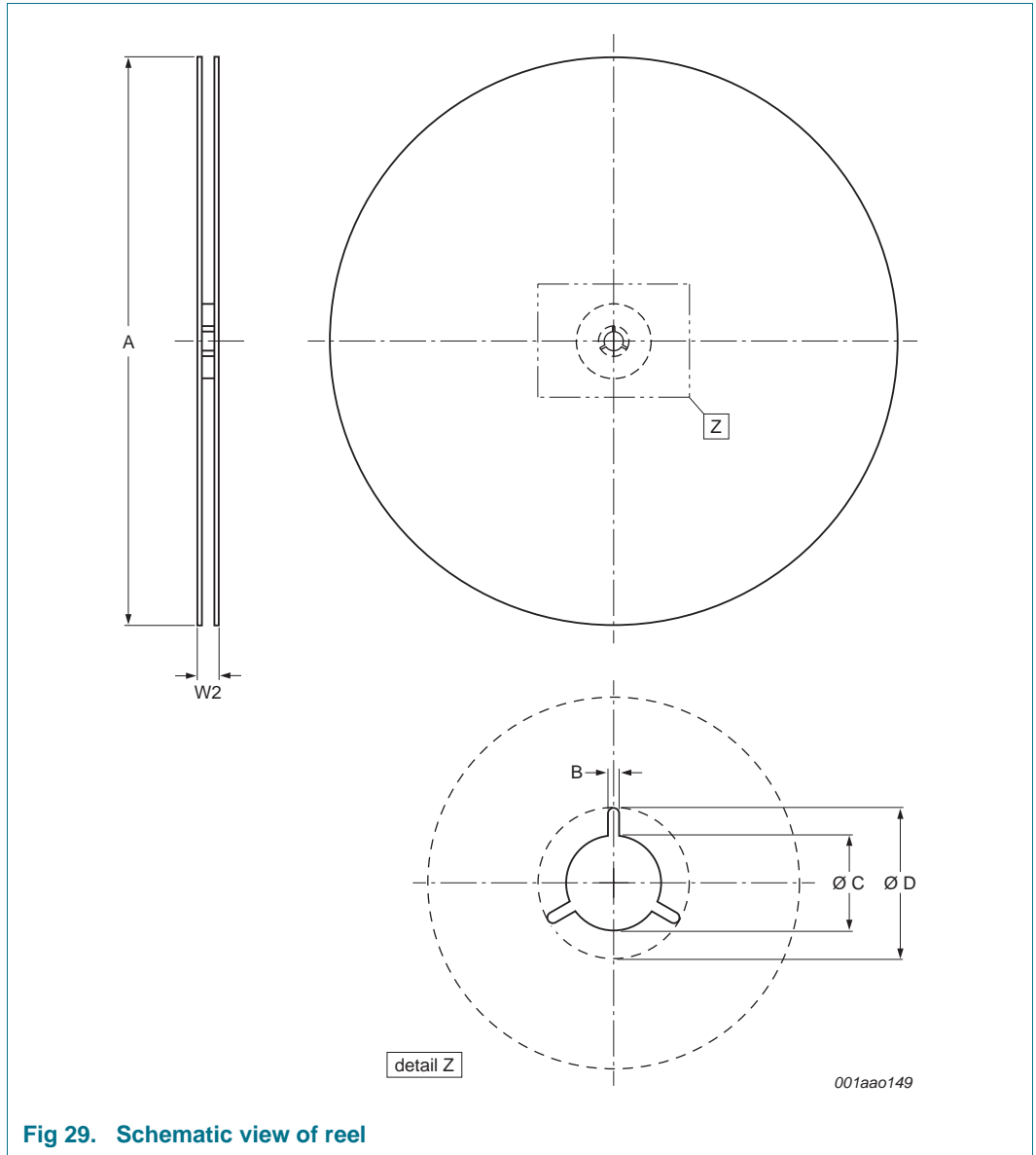


Fig 29. Schematic view of reel

Table 15. Reel dimensions
In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180	18.4	1.5	12.8	20.2

16.5 Barcode label

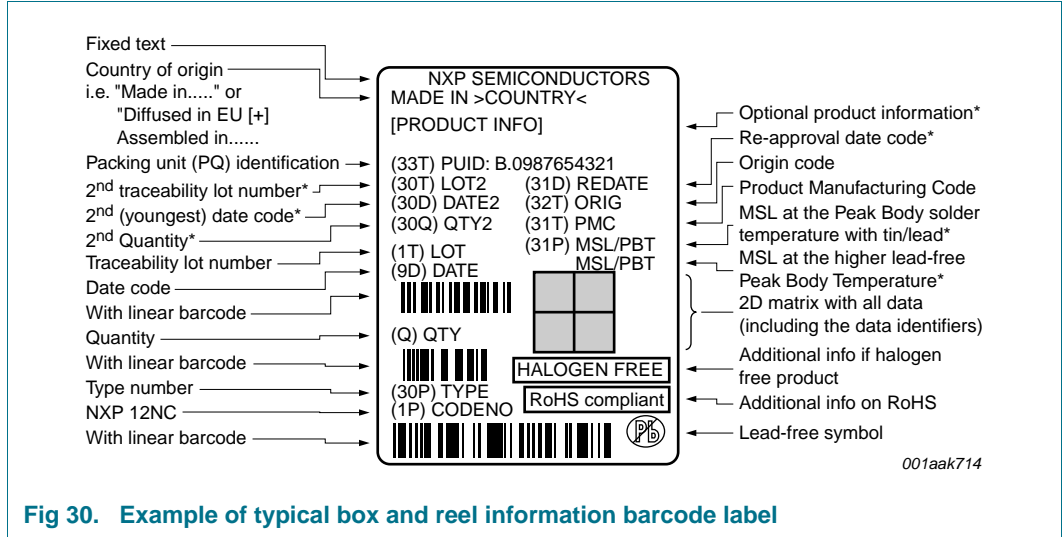


Fig 30. Example of typical box and reel information barcode label

Table 16. Barcode label dimensions

Box barcode label l x w (mm)	Reel barcode label l x w (mm)
100 x 75	100 x 75

17. Soldering of WLCSP packages

17.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 “Wafer Level Chip Scale Package” and in application note AN10365 “Surface mount reflow soldering description”.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

17.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

17.3 Reflow soldering

Key characteristics in reflow soldering are:

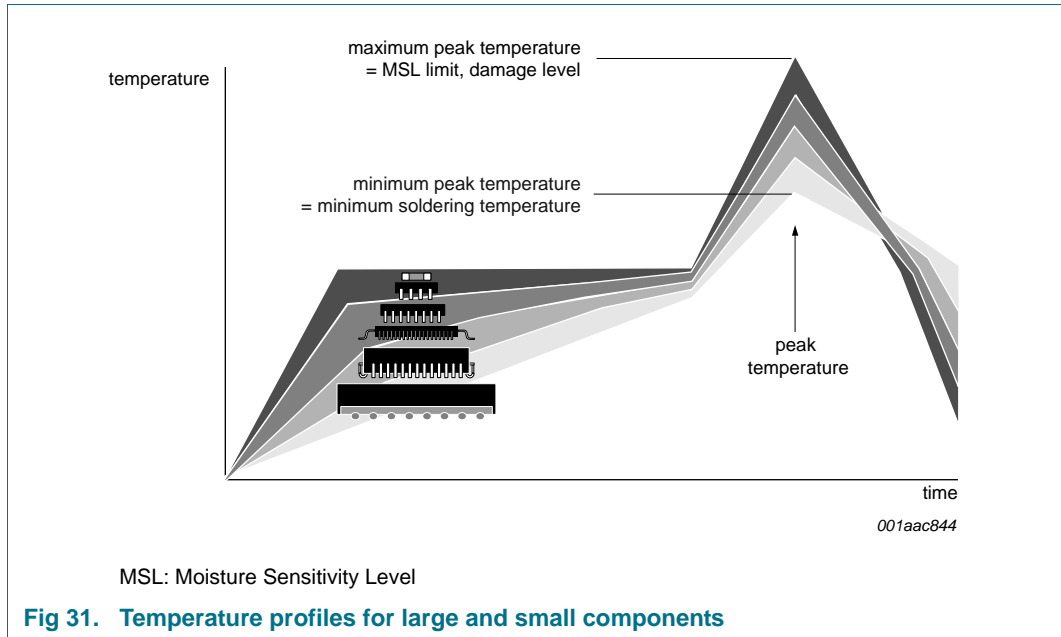
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 31](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 17](#).

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 31](#).



For further information on temperature profiles, refer to application note AN10365 “Surface mount reflow soldering description”.

17.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

17.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

17.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

17.3.4 Cleaning

Cleaning can be done after reflow soldering.

18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX20P5090 v.1	20161014	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

21. Contents

1	General description	1	19.1	Data sheet status	26
2	Features and benefits	1	19.2	Definitions	26
3	Applications	2	19.3	Disclaimers	26
4	Ordering information	2	19.4	Trademarks	27
4.1	Ordering options	2	20	Contact information	27
5	Marking	2	21	Contents	28
6	Functional diagram	3			
7	Pinning information	3			
7.1	Pinning	3			
7.2	Pin description	3			
8	Functional description	5			
8.1	$\overline{\text{EN}}$ -input	5			
8.2	Under-voltage lockout	5			
8.3	Over-voltage lockout	5			
8.4	Over-temperature protection	5			
8.5	ACK output	6			
8.6	Reverse Current Protection	6			
9	Application diagram	6			
10	Limiting values	7			
11	Recommended operating conditions	8			
12	Thermal characteristics	8			
13	Static characteristics	9			
13.1	Graphs	10			
13.2	ON resistance	13			
13.3	ON resistance test circuit and graphs	13			
14	Dynamic characteristics	14			
14.1	Waveforms and test circuit	15			
15	Package outline	17			
16	Packing information	18			
16.1	Packing method	18			
16.2	Product orientation	19			
16.3	Carrier tape dimensions	19			
16.4	Reel dimensions	20			
16.5	Barcode label	21			
17	Soldering of WLCSP packages	22			
17.1	Introduction to soldering WLCSP packages ..	22			
17.2	Board mounting	22			
17.3	Reflow soldering	22			
17.3.1	Stand off	23			
17.3.2	Quality of solder joint	23			
17.3.3	Rework	23			
17.3.4	Cleaning	24			
18	Revision history	25			
19	Legal information	26			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 October 2016

Document identifier: NX20P5090